IN THE CLAIMS:

Kindly amend claim 1 to read as follows:

Sub D

1. (Thrice Amended) A stacked semiconductor storage device comprising, in combination, a lower chip and an upper chip superimposed on a substrate, said semiconductor storage device further comprising:

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a wiring substrate having wiring patterns thereon, interposed between said lower chip and said upper chip, for relaying electric connection between bonding pads on said upper chip and bonding pads on said substrate, wherein the bonding pads on said upper chip are arranged in a line running perpendicular to a line of bonding pads on the substrate;

wherein said upper chip has an upper and a lower surface, said lower surface facing said substrate; and

wherein the bonding pads on said upper chip that connect to the bonding pads of said substrate are disposed on the lower surface of said upper chip.

REMARKS

The specification has been amended to clarify that the upper chip is upside-down, as illustrated in FIG. 3. Accordingly, claim 1 has been amended to clarify that the upper chip has an upper and a lower surface, that the lower surface faces the substrate, and that the bonding pads on the upper chip that connect to the bonding pads of the substrate are disposed on the lower surface of the upper chip. Support is found in FIG. 3 of the drawings and at page 5, line 19 to page 6, line 5. As noted therein, this arrangement makes bonding wires between the wiring sheet and the upper chip unnecessary. Neither Warren nor Bruce et al., employed to reject claim 1 under 35 USC § 103(a) teaches or suggests this construction. Moreover, this distinction is more than merely academic since, as noted in the paragraph bridging pages 5-6 of the original

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